AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1 to 22 (Cancelled)

23. (Currently Amended) A method for testing a simulation model via a graphical user interface (GUI) using a hardware-configuration database interfaced to the simulation model and to the GUI, the method comprising:

sending a query from ~~a graphical user interface~~ the GUI to ~~a~~ the hardware-configuration database, the query requesting [[,]]information ~~located within~~ associated with a hardware device simulated by the ~~a~~ simulation model, the hardware-configuration database including a location ~~locations~~ of the hardware device ~~devices~~ within the simulation model, the hardware device ~~devices representing~~ comprising functional ~~processes~~ blocks;

~~searching the functional processes to locate the information; and~~

receiving the location of the hardware device at the GUI from the hardware-configuration database;

sending commands from the GUI to the hardware device in the simulation model; and

~~directly~~ accessing ~~the~~ functional-block information of the hardware device located in the simulation model ~~from the graphical user interface~~ using the GUI, the functional-block

information being affected by the commands sent to the hardware device by the GUI. ~~without assistance from the hardware configuration database.~~

24. (Currently Amended) The method of claim 23, wherein the functional ~~processes~~ blocks represent a chip design.

25. (Previously Presented) The method of claim 24, wherein the chip design represents a processor chip.

26. (Currently Amended) The method of claim 23, further comprising combining the functional ~~processes~~ blocks into [[a]] first level ~~of~~ hierarchical relationships.

27. (Currently Amended) The method of claim 26, further comprising combining the first level hierarchical relationships into [[a]] second level ~~of~~ hierarchical relationships.

28. (Currently Amended) The method of claim 27, further comprising repeatedly combining the first level hierarchical relationships until a chip design is described.

29. (Currently Amended) The method of claim 23, wherein the simulation model is a first simulation model and the method further ~~comprising~~ comprises changing ~~the~~ hardware

descriptions stored in the hardware-configuration database to ~~forma~~ form a second simulation model.

30. (Previously Presented) The method of claim 23, wherein the query includes requests for information on a processor chip design.

31. (Currently Amended) An apparatus for testing a simulation model via a graphical user interface (GUI) using a hardware-configuration database interfaced to the simulation model and to the GUI, the apparatus comprising[[:]] circuitry to:

send a query from ~~a graphical user interface~~ the GUI to [[a]] the hardware-configuration database, the query requesting [[,]] information ~~located within~~ associated with a hardware device simulated by the ~~a~~ simulation model, the hardware-configuration database including a location ~~locations~~ of the hardware device ~~devices~~ within the simulation model, the hardware device ~~devices representing~~ comprising functional ~~processes~~ blocks;

~~search the functional processes to locate the information; and~~

receive the location of the hardware device at the GUI from the hardware-configuration database;

send commands from the GUI to the hardware device in the simulation model; and

~~directly~~ access ~~the~~ functional-block information of the hardware device located in the simulation model ~~from the graphical user interface~~ using the GUI, the functional-block

information being affected by the commands sent to the hardware device by the GUI. ~~without assistance from the hardware configuration database.~~

32. (Currently Amended) The apparatus of claim 31, wherein the functional ~~processes~~ blocks represent a chip design.

33. (Previously Presented) The apparatus of claim 32, wherein the chip design represents a processor chip.

34. (Currently Amended) The apparatus of claim 31, further comprising circuitry to combine the functional ~~processes~~ blocks into [[a]] first level ~~of~~ hierarchical relationships.

35. (Currently Amended) The apparatus of claim 34, further comprising circuitry to combine the first level hierarchical relationships into [[a]] second level ~~of~~ hierarchical relationships.

36. (Currently Amended) The apparatus of claim 35, further comprising circuitry to ~~combining~~ combine repeatedly the first level hierarchical relationships until a chip design is described.

37. (Currently Amended) The ~~repeatedly~~ apparatus of claim 31, wherein the simulation model is a first simulation model and the apparatus further ~~comprising~~ comprises circuitry to change the hardware descriptions stored in the database to form a second simulation model.

38. (Previously Presented) The method of claim 31, wherein the query includes requests for information on a processor chip design.

39. (Currently Amended) An article comprising a machine-readable medium that stores executable instructions for testing a simulation model via a graphical user interface (GUI) using a hardware-configuration database interfaced to the simulation model and to the GUI, the instructions causing a machine to:

send a query from ~~a graphical user interface~~ the GUI to [[a]] the hardware-configuration database, the query requesting [[,]]information ~~located within~~ associated with a hardware device simulated by the [[a]] simulation model, the hardware-configuration database including a location ~~locations~~ of the hardware device ~~devices~~ within the simulation model, the hardware device ~~devices representing~~ comprising functional ~~processes~~ blocks;

~~search the functional processes to locate the information; and~~

receive the location of the hardware device at the GUI from the hardware-configuration database;

send commands from the GUI to the hardware device in the simulation model; and

~~directly~~ access ~~the~~ functional-block information of the hardware device located in the simulation model ~~from the graphical user interface~~ using the GUI, the functional-block information being affected by the commands sent to the hardware device by the GUI. ~~without assistance from the hardware configuration database.~~

40. (Currently Amended) The article of claim 39, wherein the functional ~~processes~~ blocks represent a chip design.

41. (Previously Presented) The article of claim 40, wherein the chip design represents a processor chip.

42. (Currently Amended) The article of claim 39, wherein the medium further comprises ~~instruction~~ instructions causing a machine to combine the functional ~~processes~~ blocks into [[a]] first level ~~of~~ hierarchical relationships.

43. (Currently Amended) The apparatus of claim 42, wherein the medium further comprises ~~instruction~~ instructions causing a machine to combine the first level hierarchical relationships into [[a]] second level ~~of~~ hierarchical relationships.

44. (Currently Amended) The apparatus of claim 43, wherein the medium further comprises ~~instruction~~ instructions causing a machine to combine repeatedly the first level hierarchical relationships until a chip design is described.

45. (Currently Amended) The ~~repeatedly~~ article of claim 39, wherein the simulation model is a first simulation model and the medium further comprises ~~instruction~~ instructions causing a machine to change ~~the~~ hardware descriptions stored in the hardware-configuration database to form a second simulation model.

46. (Previously Presented) The method of claim 39, wherein the query includes requests for information on a processor chip design.